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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,733	03/31/2004	Van Hoa Lee	AUS920040057US1	7203

35525 7590 05/02/2006

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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,733	LEE, VAN HOA	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/814,733 has a total of 20 claims pending in the application; there are 3 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. OBJECTIONS TO THE SPECIFICATION

CLAIM OBJECTIONS

4. **Claims 1 and 7** are objected to because of the following informalities:

As per **claims 1 and 7**, the words "upper most" (claim 1, line 19 and claims 7, line 14) and "lower most" (claim 7, line 11) are believed to be "uppermost" and "lowermost" and have been treated as such for the rest of this office action

Appropriate correction is required.

IV. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 7-14** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

7. As per **claims 7-14**, these claims recite the limitation of "a computer readable medium" which, Applicant's specification defines as "transmission-type media, such as digital and analog communications links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions" (page 13, lines 23-30). Therefore, claims 7-14 are directed to non-statutory subject matter as these claims recite nothing more than a transmission media to transfer signals which are defined as physical characteristics of a form of energy, such as frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are nonstatutory phenomena. Moreover, it does not appear that a claim reciting a signal encoded with function descriptive material falls within any of the categories of patentable subject matter set forth 35 U.S.C. 101.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1-5, 7-13, 15-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harvey et al. (US 6,061,773) in view of Stine et al. (US 6,629,111).

10. As per **claims 1, 7, 15 and 20**, Harvey discloses

"A method/computer program product/system of supporting memory addresses with holes, the method comprising:" as **["the present system processes requests for allocation of virtual memory such that the inaccessible gap is avoided, and the requester is provided with a starting address of a virtually contiguous range of allocated virtual memory which is not encompassing or within the inaccessible gap" (Column 24, lines 26-31)]**

"a memory" **[With respect to this limitation, Harvey discloses "memory 14" (Figure 1)]**

"a data set" **[Harvey discloses this limitation as "shared page table entries 26," and "private page table entries" 30, 34 and 38 (Figure 1)]**

"a set of instructions" **[With respect to this limitation, Harvey discloses that "Memory management software maintains tables of mapping information (page tables) that keep track of where each page of virtual addresses is located in physical memory. The CPU uses this mapping information when it translates virtual addresses to physical addresses" (Column 1, lines 1-35) "memory management unit 20" which is responsible for address translation (Figure 1 and Column 6, lines 10-14 and 40-53)]**.

"a processor" **[With respect to this limitation, Harvey discloses "CPU 10" (Figure 1 and Column 1, lines 15-35)]**

"virtualizing a first physical address range allocated for system memory for an operating system run by a processor configured to support logical partitioning to produce a first logical address range;" **[With respect to this limitation, Harvey discloses "virtual address space 450" having a range mapped from address 00000000.00000000 "lowest virtual address 452" to address 00000400.00000000 "gap base 460" (Figure 19 and Column 22, lines 60-66)]**

"virtualizing a second physical address range allocated for system memory for the operating system to produce a second logical address range, wherein the first physical address range and the second physical address range are non-contiguous and the first logical address range and the second logical address range are contiguous;" **[With respect to this limitation, Harvey discloses "virtual address space 450" having a range mapped from address FFFFFC00.00000000 "gap limit 462" to address FFFFFFFF.FFFFFFFF "highest virtual address 454" (Figure 19 and Column 22, lines 60-66) and explains having a "virtually contiguous address space" (Figure 15 and Column 19, lines11-18)]**. Harvey also discloses having an address range "wherein a lowermost logical address of the third logical address range exceeds a respective upper most logical address of the first and second logical address ranges" **["inaccessible gap 456" which is intermediate to a first logical range and a second logical range (Figure 19 and Columns 22-23, lines 60-67 and 1-29)]**.

Harvey does not disclose expressly "virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range."

Stine discloses "virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range" as **["a memory allocation scheme which may be used to conserve memory that is to be accessed by one or more clients (e.g. computers or applications)" (Column 5, lines 5-8) and explains identifying regions of memory which may normally go unused "memory holes" and allocating these regions to clients (Column 3, lines 8-56, Figure 10 and Column 10, lines 9-29)]**.

Harvey et al. (US 6,061,773) and Stine et al. (US 6,629,111) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art modify the memory virtualization system which includes a memory gap/hole as taught by Harvey and further map memory access operations within this memory hole as taught by Stine.

The motivation for doing so would have been because Stine discloses that allocating "memory holes" to processes or applications allows **[the conservation of physical memory as "the corresponding number of pages required in virtual memory are minimized;" also facilitating the utilization of memory as "when a hole in a memory segment already containing data is used, a new TLB entry need not be**

created since the hole is mapped in an entry in the memory segment list" (Column 4, lines 6-24)].

Therefore, it would have been obvious to combine Stine et al. (US 6,629,111) with Harvey et al. (US 6,061,773) for the benefit of creating a memory virtualization system to obtain the invention as specified in claim 1.

11. As per **claims 2 and 16**, the combination of Harvey and Stine discloses "The method/system of claims 1 and 15," **[See rejection to claims 1 and 15 above]** wherein "the dataset is a mapping table;" wherein "the steps of virtualizing the first physical address range, the second physical address range, and the memory mapped input/output physical address range comprises maintaining a mapping table that defines physical addresses and corresponding logical addresses" **[With respect to this limitation, Harvey discloses a "page table" mapping physical memory to logical memory (Figure 8 and Columns 11-12, lines 65-67 and 1-17)]**. Stine also discloses this limitation as **["TLB 104" which is used to translate virtual addresses to physical addresses (Figure 1B and Column 1, lines 39-67)]**.

12. As per **claims 3 and 8**, the combination of Harvey and Stine discloses "The method/computer program of claims 2 and 7," **[See rejection to claims 2 and 7 above]** "wherein maintaining the mapping table further comprises maintaining the mapping table in a physical address space allocated to one of the first and second physical address ranges, and wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges" **[With respect to this limitation, Harvey discloses an embodiment in which "the set of process page table entries includes a page table entry mapping the page table itself to pages of physical**

memory" (Column 4, lines 1-3) and explains that "exactly as much virtual memory as is necessary is reserved for mapping the page table entries, regardless of page size of page table depth in a specific implementation" (Figures 15 and 17 and Column 21, lines 36-40)].

13. As per **claim 4**, the combination of Harvey and Stine discloses "The method of claim 1," **[See rejection to claim 1 above]** "wherein the third logical address range is non-contiguous with the first logical address range and the second logical address range" **[With respect to this limitation, Stine discloses that upon allocation, memory segments include one or more pages that may contain unused portions which comprise "memory holes" (Column 2, lines 39-65 and Figure 2); therefore, allocated memory may contain memory holes (equivalent to "the third logical address space" as claimed by applicant) anywhere within an address space, which means they are not be contiguous with allocated memory blocks].**

14. As per **claim 5**, the combination of Harvey and Stine discloses "The method of claim 1," **[See rejection to claim 1 above]** "further comprising: allocating a portion of at least one of the first physical address range and the second physical address range for a logical partitioning management software layer" **[With respect to this limitation, Harvey discloses "memory management unit 20" which is responsible for address translation (Figure 1 and Column 6, lines 10-14 and 40-53)].**

15. As per **claims 9 and 18**, the combination of Harvey and Stine discloses "The computer program product/system of claims 8 and 15," **[See rejection to claims 8 and 15 above]** "wherein the mapping table is maintained in at least one of the first and second physical address ranges" **[With respect to this limitation, Harvey discloses that a**

virtual memory space may be divided into "shared address" and "private address" spaces wherein "page table entries within a page table may be located in either process private or share space" (Column 2, lines 3-5)].

16. As per **claims 10 and 17**, the combination of Harvey and Stine discloses "The computer program product/system of claims 7 and 15," **[See rejection to claims 7 and 15 above]** "wherein the second instructions provide logical partitioning functionality" **[With respect to this limitation, Harvey discloses that "Memory management software maintains tables of mapping information (page tables) that keep track of where each page of virtual addresses is located in physical memory. The CPU uses this mapping information when it translates virtual addresses to physical addresses" (Column 1, lines 1-35) "memory management unit 20" which is responsible for address translation (Figure 1 and Column 6, lines 10-14 and 40-53)].**

17. As per **claims 11 and 19**, the combination of Harvey and Stine discloses "The computer program product/system of claims 7 and 15," **[See rejection to claims 7 and 15 above]** "wherein the second instructions are maintained in at least one of the first and second physical address ranges" **["Memory management software maintains tables of mapping information (page tables) that keep track of where each page of virtual addresses is located in physical memory. The CPU uses this mapping information, when it translates virtual addresses to physical addresses" (Column 1, lines 1-35) "memory management unit 20" which is responsible for address translation (Figure 1 and Column 6, lines 10-14 and 40-53) and explains that a virtual memory space may be divided into "shared address" and "private address" spaces wherein "page table entries within a page table may be located in either process private or share**

space" (Column 2, lines 3-5) as having data stored anywhere in a memory system except in an inaccessible gap].

18. As per **claim 12**, the combination of Harvey and Stine discloses "The computer program product of claim 7," **[See rejection to claim 7 above]** "wherein the second instructions interface an operating system with input and output devices of a data processing system" **[With respect to this limitation, Stine discloses "a memory allocation scheme which may be used to conserve memory that is to be accessed by one or more clients (e.g. computers or applications)" (Column 5, lines 5-8) and explains identifying regions of memory which may normally go unused "memory holes" and allocating these regions to clients (Column 3, lines 8-56, Figure 10 and Column 10, lines 9-29)]**.

19. As per **claim 13**, the combination of Harvey and Stine discloses "The computer program product of claim 12," **[See rejection to claim 12 above]** "wherein the second instructions present a contiguous logical address range comprising the first and second logical address ranges to the operating system" **[With respect to this limitation, Harvey discloses that "Memory management software maintains tables of mapping information (page tables) that keep track of where each page of virtual addresses is located in physical memory. The CPU uses this mapping information when it translates virtual addresses to physical addresses" (Column 1, lines 1-35) "memory management unit 20" which is responsible for address translation (Figure 1 and Column 6, lines 10-14 and 40-53)]**.

20. **Claims 6 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harvey et al. (US 6,061,773) in view of Stine et al. (US 6,629,111) as applied to claims **1-5, 7-13 and 15-20** above, and further in view of Yazdy et al. (US 6,256,710).

21. As per **claims 6 and 14**, the combination of Harvey and Stine discloses "The method of claims 1 and 8," **[See rejection to claims 1 ad 8 above]** but does not expressly disclose having a "memory mapped input/output physical address range is allocated for cache inhibited addresses."

Yazdy discloses having a "memory mapped input/output physical address range is allocated for cache inhibited addresses" as **[a software system in which "it may be desirable in certain cases to define areas of main memory as being non-cacheable" and explains "declaring one or more ranges of memory as non-cacheable" (Figure 1 and Column 2, lines 23-41). Note that figure 1 shows a block of "non-cacheable data" placed between two blocks of cacheable data as claimed by Applicant]**.

Harvey et al. (US 6,061,773), Stine et al. (US 6,629,111) and Yazdy et al. (US 6,256,710) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art modify the memory virtualization system which includes a memory gap/hole as taught by Harvey, further map memory access operations within this memory hole as taught by Stine and further use a gap/hole to store cache-inhibited data, as taught by Yazdy.

The motivation for doing so would have been because Yazdy discloses that allocating a memory block for cache-inhibited address **["by providing software with the**

opportunity to define its own regions of non-cacheable main memory, cache performance can be optimized by looking to the cache for ranges of main memory which are more likely to be reaccessed" (Column 2, lines 54-58)].

Therefore, it would have been obvious to combine Yazdy et al. (US 6,256,710), Stine et al. (US 6,629,111) and Harvey et al. (US 6,061,773) for the benefit of creating a memory virtualization system to obtain the invention as specified in claim 6.

VI. RELEVANT ART CITED BY THE EXAMINER

22. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

23. The following references teach cache memory systems having inhibited address spaces.

U.S. PATENT NUMBER

US 5,706,464

US 6,564,299

US 5,297,270

US 4,991,082

24. The following references teach memory-mapped I/O.

U.S. PATENT NUMBER

US 5,581,768

US 2003/0177332

US 2003/0188062

25. The following reference teaches file allocation tables with holes.

U.S. PATENT NUMBER

US 5,819,298

26. The following reference teaches having I/O segments distributed non-contiguously.

U.S. PATENT NUMBER

US 5,548,746

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

27. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

28. Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

30. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 18, 2006

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER